What is claimed is:

1. A memory device, comprising:

a substrate with a plurality of deep trenches, wherein the deep trenches in the adjacent rows are staggered;

a plurality of deep trench capacitors disposed in the deep trenches of the substrate respectively;

a plurality of control gates disposed on the deep trench capacitors respectively;

a plurality of word lines disposed on the control gates respectively along a first direction, each word line being electrically coupled to the control gate thereunder;

a plurality of diffusion regions disposed in the substrate and surrounding the deep trenches respectively to serve as sources of vertical transistors, wherein each diffusion region is electrically connected to the surrounding deep trench capacitor;

a plurality of active areas disposed on the rows of the control gates respectively along a second direction, wherein the regions where each active area overlaps the control gates have at least one indentation; and

a plurality of drains disposed in the active areas beside each word line.

2. The memory device as claimed in claim 1, wherein the first direction is essentially perpendicular to the second direction.

3. The memory device as claimed in claim 1, wherein each active area has normal portions and recessed portions, each recessed portion is disposed between two normal portions, and each of the recessed portions overlaps one of the control gates thereunder and has an indentation on both sides.

4. The memory device as claimed in claim 3, wherein each normal portion has a first width, and each recessed portion has a second width smaller than the first width.

5. The memory device as claimed in claim 4, wherein each normal portion has a lateral surface on both side, and each recessed portion has two slanted surfaces and a plane surface, and, relative to the lateral surface, each plane surface has a width diminution.

6. The memory device as claimed in claim 5, wherein the angle of the lateral surface relative to the slanted surface is 135°.

7. The memory device as claimed in claim 1, wherein the word lines are composed of polysilicon.

8. The memory device as claimed in claim 1, further comprising a plurality of bit lines disposed on

the active areas, and electrically coupled to the drains thereunder respectively.

9. A method for forming memory device, comprising:
forming a plurality of deep trenches in a substrate;
forming a deep trench capacitor in each deep trench;
forming a diffusion region surrounding each deep trench capacitor in the substrate;
forming a control gate on each deep trench capacitor;
forming a word line on each control gate along a first direction;
forming an active area corresponding to one row of the control gates, wherein the regions overlapping the active area and the control gates have an indentation on both sides; and
forming two drains on the active area beside the word line using the word line as a mask.

10. The method as claimed in claim 9, wherein each active area have normal portions and recessed portions, each recessed portion is disposed between two normal portions, and each of the recessed portions overlaps one of the control gates thereunder and has an indentation on both sides.

11. The method as claimed in claim 10, wherein each normal portion has a first width, and each recessed portion has a second width smaller than the first width.

12. The method as claimed in claim 11, wherein each normal portion has a lateral surface on both sides, and

each recessed portion has two slanted surfaces and a plane surface, and, relative to the lateral surface, each plane surface has a width diminution.

13. The method as claimed in claim 12, wherein the angle of the lateral surface relative to the plane surface is 135°.

14. The method as claimed in claim 9, further comprising a step of forming an isolation layer between each deep trench capacitor and each control gate.

15. The method as claimed in claim 9, further comprising a step of forming a bit line on the active area, wherein the bit line is electrically coupled to the drains in the active areas by bit line contacts.